SIEMENS

PCM 2-Channel-Codec SM 61A/S 291, SM 61A/S 291A SM 61B/S 291A

Edition October 1978

SIEMENS AKTIENGESELLSCHAFT

Published by Siemens AG, Bereich Bauelemente, Produkt-Information, Balanstraße 73, D-8000 München 80.

For questions on technology, delivery and prices please contact the Offices of Siemens Aktiengesellschaft in the Federal Republic of Germany and Berlin (West) or the Siemens Companies and Representatives abroad (see list of Sales Offices).

PCM CODEC SM 61A/S 291

Preliminary specifications

Features

- Two–channel codec as a two-chip system:
  SM 61A in NMOS-, S 291 in bipolar technology
- Codec for two analogue channels at 8 kHz sampling, or one analogue channel at 16 kHz sampling
- A-companding to CCITT G 711
- PCM interface 2.048 MHz serially
- Digital interfaces TTL-compatible
- Supply voltages: +12 V, +5 V, –5 V
- Temperature-compensated voltage reference on the chip
- Automatic offset-balance of the comparator
- Low power consumption: 125 mW/channel
- Only one frame-synchronous pulse required

The **SIEMENS CODEC**-system SM 61A/S 291 has been designed for the **co**ding and **dec**oding of analogue signals in the speech frequency range, for use in time multiplex systems with pulse code modulation (PCM 30/32). Accuracy and reliability of the codec-functions require a suitable technology without trimming in the fabrication process. This is why SIEMENS uses the appropriate bipolar technology for integrating the codec's analogue functions (circuit S 291) and the NMOS technology for realization of its control logic and digital functions (circuit SM 61A). Designing the codec for two channels reduces the device count to one IC per channel.

The NMOS IC comprises the input- and output-sampling circuits, the D/A converter, the PCM-converter-register and the timing control. The bipolar IC contains the reference-current generator, the current-voltage-converter, the comparator and two additional operational amplifiers.

Main applications

Transmission systems:

- PCM 30/32-system at 2.048 Mbits

Switching systems:

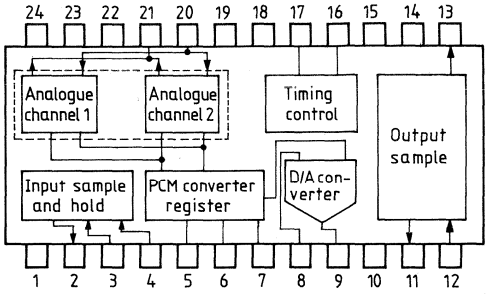
- Digital subscriber circuit
- Single-stage concentrator (32 switched channels)
- Single-stage switching matrix for PABX and PAX telephone systems (32 switched channels)

General signal processing:

- speech digitalization

Pin assignment

NMOS Circuit SM 61A

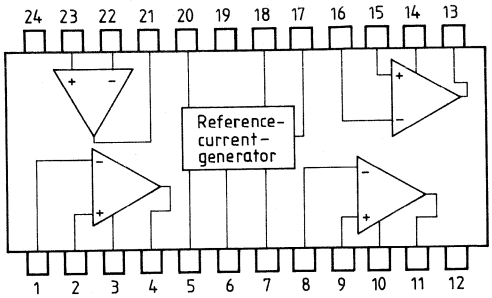


Pin No	Name	Function
1	V_{SS}	Supply voltage −5 V ±5% Power consumption relative to digital ground 11 mW
2	TEM	Connection for the hold-capacitor (3.3 nF). Mutual connection of the two input sample circuits (mid-point); alternately, the sample values of analogue channels 1 and 2 and the positive input of the comparator are connected to this point
3	TE1	Input sample and hold for analogue channel 1 = input for the analogue signal of channel 1 to be digitized; sample time 4 µs.
4	TE2	As above, channel 2
5	KE	Input of comparator decision, to be utilized by the converter-register (successive approximation)
6	VA	Polarity of the analogue sample, to be utilized by the reference current generator
7	ANA	Automatic zero balance, compensates the comparator offset down to 0.2 mV
8	IE	Reference-current input to the D/A converter, polarity switched by VA
9	IA	Weighting current of D/A conversion, for utilization by the current/voltage converter
10	OA	Analogue ground, reference for all analogue signals
11	TA1	Output sampling circuit for analogue channel 1 = output of the decoded value for analogue channel 1; PAM signal 4 µs; connection for a hold-capacitor of 2.2 nF used for generating a staircase function

Pin No	Name	Function
12	TAM	Mutual connection of the two output-sample-circuits (mid-point). At this point the output of the current/voltage converter is to be connected, i.e. the decoded analogue value is applied here and sampled for channels 1 and 2
13	TA2	Output sample circuit for analogue channel 2 = output of the decoded value for analogue channel 2; connection for a hold-capacitor of 2.2 nF
14	V_{GG}	Supply voltage +12 V ± 5% Power consumption relative to digital ground 125 mW
15	V_{DD}	Supply voltage +5 V ± 5% Power consumption relative to digital ground 50 mW
16	$\overline{SYE}$	Input for the synchronizing pulse which controls the converter. Duration at least one period of the 2.048 MHz clock. Negative going edge synchronous with start of channel.
17	T	2.048 MHz clock = frequency of bit sequence; Pulse/pause ratio 1:1
18	$\overline{EE1}$	O-sensitive input for the receive pulse of analogue channel 1. Duration of pulse is 8 clock periods of the 2.048 MHz clock, at a channel pattern ≙ 8 bit PCM. Function: Transfer of the PCM-word into the intermediate register of channel 1 through PCM-E in the order of decreasing significance
19	$\overline{EE2}$	As above, channel 2
20	PCME	Reception of arriving PCM information in nini-code (even numbered bits inverted), serially at 2.048 MHz. Channel allocation determined by receive control pulse. $\overline{EE1}$ or $\overline{EE2}$, or $\overline{SYE}$ respectively in the case of short-way operation. Tristate function.
21	PCMA	Output of the PCM-information in nini-code, serially at 2.048 MHz; bit sequence in the order of decreasing signifcance. Channel allocation determined by send control pulse $\overline{SE1}$ or $\overline{SE2}$, or $\overline{SYE}$ respectively in the case of short-way operation. Tristate function.
22	$\overline{SE1}$	O-sensitive input for the send-pulse of analogue channel 1. Duration of pulse is 8 clock periods of the 2.048 MHz clock, at a channel pattern of ≙ 8 bit PCM. Function: Transfer of the PCM-word, in the order of decreasing significance, from the intermediate register to PCMA.
23	$\overline{SE2}$	As above, channel 2
24	O_D	Digital ground, reference for all digital signals

Pin assignment

bipolar circuit S 291



Pin No	Name	Function	
1	WNE1	Inverting input of the OP1	Use: Matching of analogue channel 2
2	WPE1	Non-inverting input of the OP1	
3	WK1	Compensation of the OP1	
4	WA1	Output of the OP1	
5	IA2	Output of the reference current generator for utilization by the D/A-converter	
6	IA1	Output of the reference current generator, IA1 = –IA2	
7	IK	Compensation of the reference current generator	
8	WNE2	Inverting input of the OP2	Use: Matching of analogue channel 1
9	WPE2	Non-inverting input of the OP2	
10	WK2	Compensation of the OP2	
11	WA2	Output of the OP2	
12	$-V_S$	Supply voltage –5 V ± 5%. Power consumption relative to ground 25 mW	
13	WA3	Output of the OP3	Use as current/ voltage converter for weighting – current
14	WK3	Compensation of the OP3	
15	WPE3	Non-inverting input of the OP3	
16	WNE3	Inverting input of the OP3	

Pin No	Name	Function
17	URA	Output of the reference voltage, URA = 1.25 V temperature-compensated
18	URE	Input of the reference current generator. Resistor between URA and URE determines the reference-current
19	O_S	Ground Reference for all signals
20	VE	Input of sign information (TTL-compatible), at H-level: IA1 >0 at L-level: IA1 <0
21	KA	Output of comparator decision
22	KNE	Inverting input of the comparator
23	KPE	Non-inverting input of the comparator
24	$+V_S$	Supply voltage +5 V ± 5% Power consumption relative to ground 25 mW

Maximum ratings:

NMOS circuit SM 61A

Supply voltage (relative to V_{SS})		±20	V
Functional range		$V_{nominal}$ ± 10%	V
Ambient temperature	T_{amb}	−25 to +75	°C
Storage temperature	T_s	−60 to +150	°C
Total power dissipation	P_{tot}	300	mW

Bipolar circuit S 291

Supply voltage	V_S	± 10	V
Output current	I_{WA}	± 30	mA
Input difference voltage	V_{WDE}	± 8	V
Input voltage for OP's and comparator		± 10	V
for sign		± 4 to ± 10	V
Functional range		± 4 to ± 10	V
Ambient temperature in operation	T_{amb}	−25 to +75	°C
Junction temperature	T_j	125	°C
Heat resistance	SU	120	K/W
Total power dissipation	P_{tot}	600	mW
Storage temperature	T_s	−60 to +150	°C

Operating characteristics ($V_{SS} = -V_S = -5$ V, $V_{DD} = +V_S = +5$ V, $V_{GG} = +12$ V, $T_{amb} = 25$°C)

NMOS circuit SM 61A

Analogue value range	± 2.5	max.	V
Input level	TTL compatible		
Output level	1 TTL load	200	pF
Input and output capacitance	10	max.	pF
Lowest step-increment	1.2		mV
Auto-zero	0.4	max.	mV
Output delay	100		ns
Input hold time	100		ns
Time difference between T and $\overline{SYE}$	± 50		ns
Resistance of sampling switch	<200 Ω;	>20 MΩ	
Cross talk attenuation	80		dB

Bipolar circuit S 291

Reference current generator		min	typ	max	unit
Reference voltage	V_{RA}	1.2	1.25	1.3	V
Temp. coeff. of V_{RA}	V_{RA}			300	ppm K^{-1}
Input offset voltage	V_{ZE}			± 5	mV
Impedance of the reference current	R_{IA1}		10		MΩ
outputs	R_{IA2}		10		MΩ
Signs:					
Input current ($V_{VE} = 0$)	$-I_{VE}$		3	10	μA
H-input voltage	V_{VEH}	2			V
L-input voltage	V_{VEL}			0.8	V

Comparator

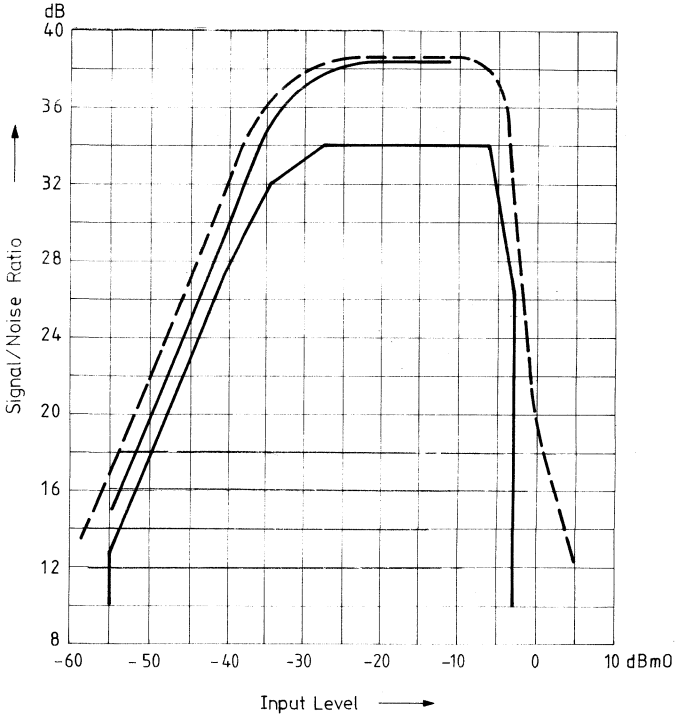
		min	typ	max	unit
Input current	I_{KE}		10	50	nA
Input null voltage	V_{KE}			± 5	mV
H-output current	I_{KAH}	200			µA
L-output current	I_{KAL}			10	mA
H-output voltage	V_{KAH}	4			V
L-output voltage	V_{KAL}			−4	V
Hysteresis	V_{KEHY}		0.25	0.4	mV
Voltage gain	A_V		100		dB
Delay time	t_{PLH}		0.8		µs
Input synchronism range		± 3			V

Operational amplifier

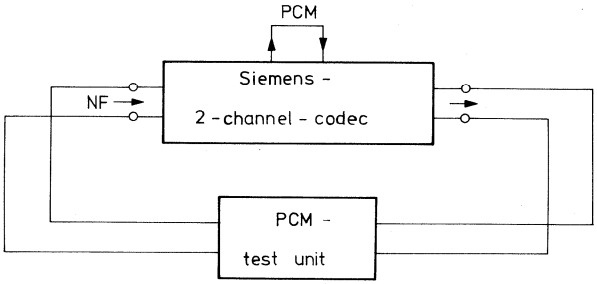
Input null voltage	V_{WEOS}			± 5	mV
Input current	I_{WE}		10	30	nA
Input null current	I_{WEOS}			10	nA
Modulation range (R_L = 150 Ω)	V_{WA}	−2.5		2.5	V
Input synchronism range	V_{WEG}	−2.5		2.5	V
Voltage gain	A_V		75		dB
Transition of output voltage 1% faults, inverter with A_V = 0 dB, voltage change V_E = 20 mV)	t_r		0.5		µs
Rising edge	dV_{WA}/dt		2		V/µs

Code SM 61A / 291 system

Signal-noise ratio	S/N	2 dB above tolerance -scheme according to figure 1	dB
Level dependence of rest attenuation		Within limits of tolerance-scheme according to figure 2	dB
Frequency dependence of rest attenuation		Within limits of tolerance-scheme according to figure 3	dB
Quiescent noise		>−65	dB mO
Cross talk		>−65	dB mO
Clock frequency		2.048	MHz
Power consumption		250	mW



— — Theoretical Value
——— Measured Curve
——— Recommended S/D Tolerance Scheme (CCITT).



Channel Quiscent Noise – 70.9 dB mO

Figure 1: **Signal/Noise ratio according to CCITT**

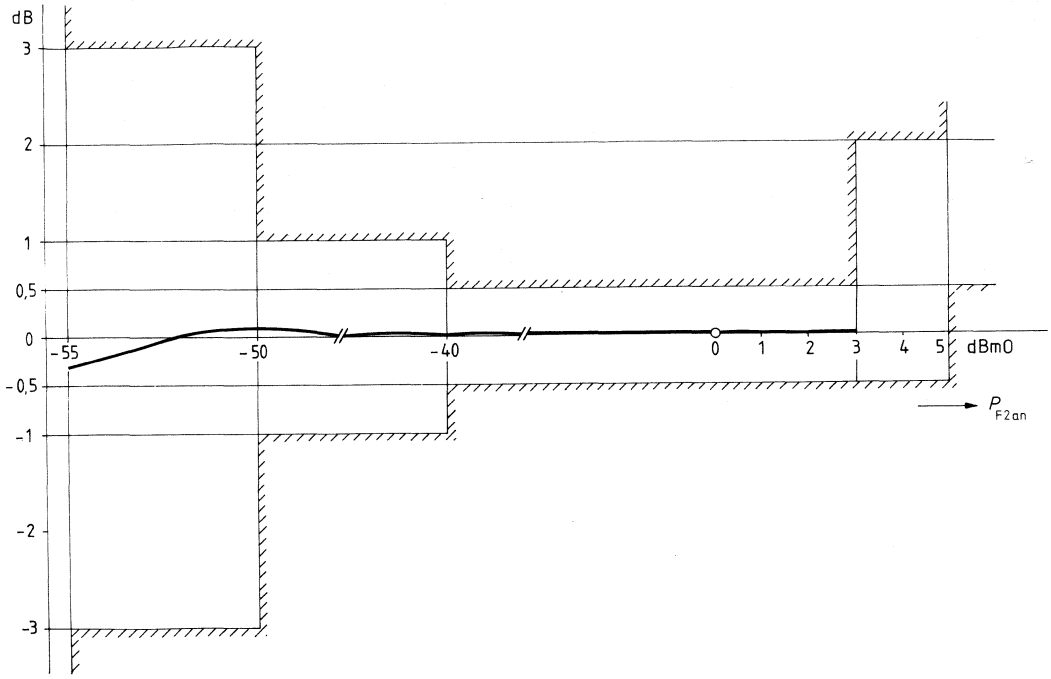


Figure 2: **Level-dependence of the rest-attenuation**

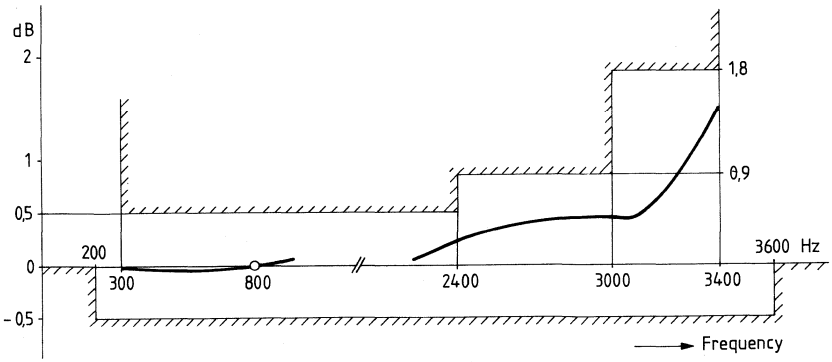


Figure 3: **Frequency-dependence of rest-attenuation**

Description of function

General:

In Pulse Code Modulation transmission systems, the low frequency band-limited voice signal mixture is sampled at 8 kHz and converted to an 8-bit PCM code, corresponding to 256 quantification steps. Consequently the coding and decoding of two channels are performed within one clock period of 1/8 kHz = 125 µs in the Siemens codec. The time multiplex system PCM 30/32 specified by CCITT, using a bitrate of 2.048 Mbit/s, therefore permits time-multiplexing of 30 telephone- and 2 control channels.

CCITT (G. 711) has specified a 13-segment companding characteristic for the analogue value and PCM-code correlation (A-companding), which the Siemens 2-channel codec conforms to (fig. 4). Accordingly, the first bit is determined by the polarity of the signal. Bits 2, 3 and 4 indicate, in which of the eight sections of the characteristic the signal is located. Finally, the last four bits (bit 5 . . . 8) define one of the 16 intervals of the relevant section of the sample value. Because the four sections around the zeropoint have the same rate of increment and consequently the same resolution (segment 7), there are 13 segments in the total characteristic with rates of increment in the ratio 2 : 1, yielding for small signal amplitudes a correspondingly higher resolution than for large amplitudes.

External connections:

Figure 5 shows the external connections of the two circuits with the evaluation board now offered by Siemens, and which will serve as a basis for the following discussion of the codec functions.

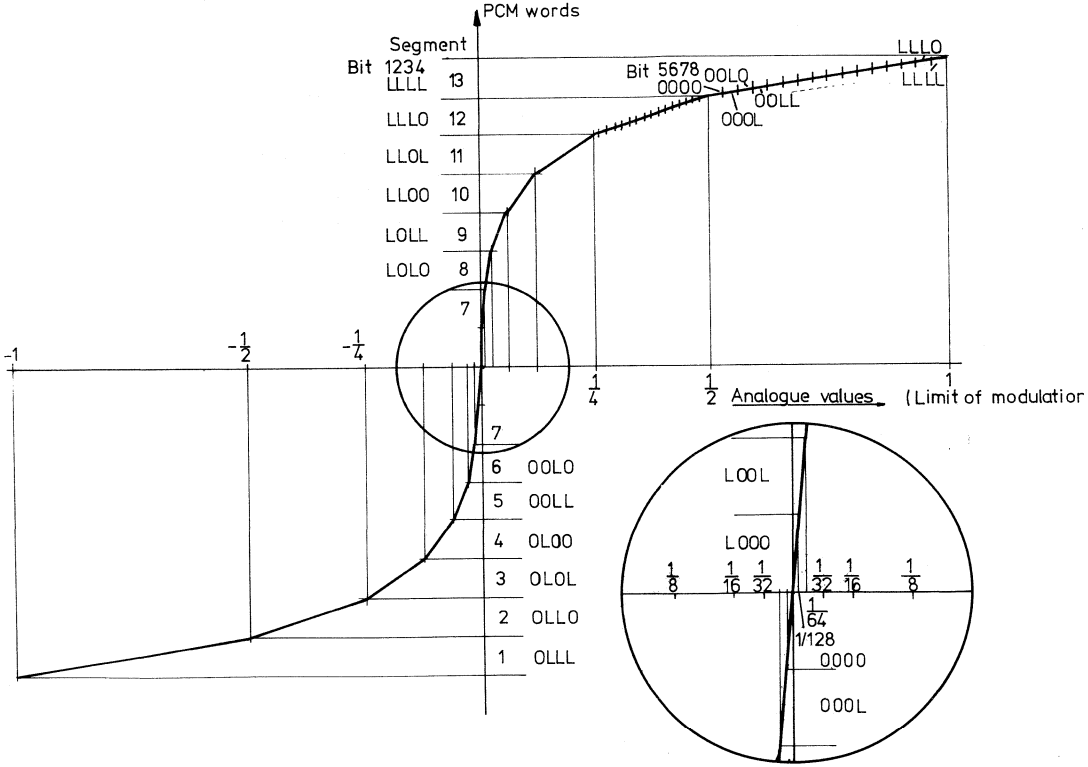


Figure 4: **Segment-compander characteristic**

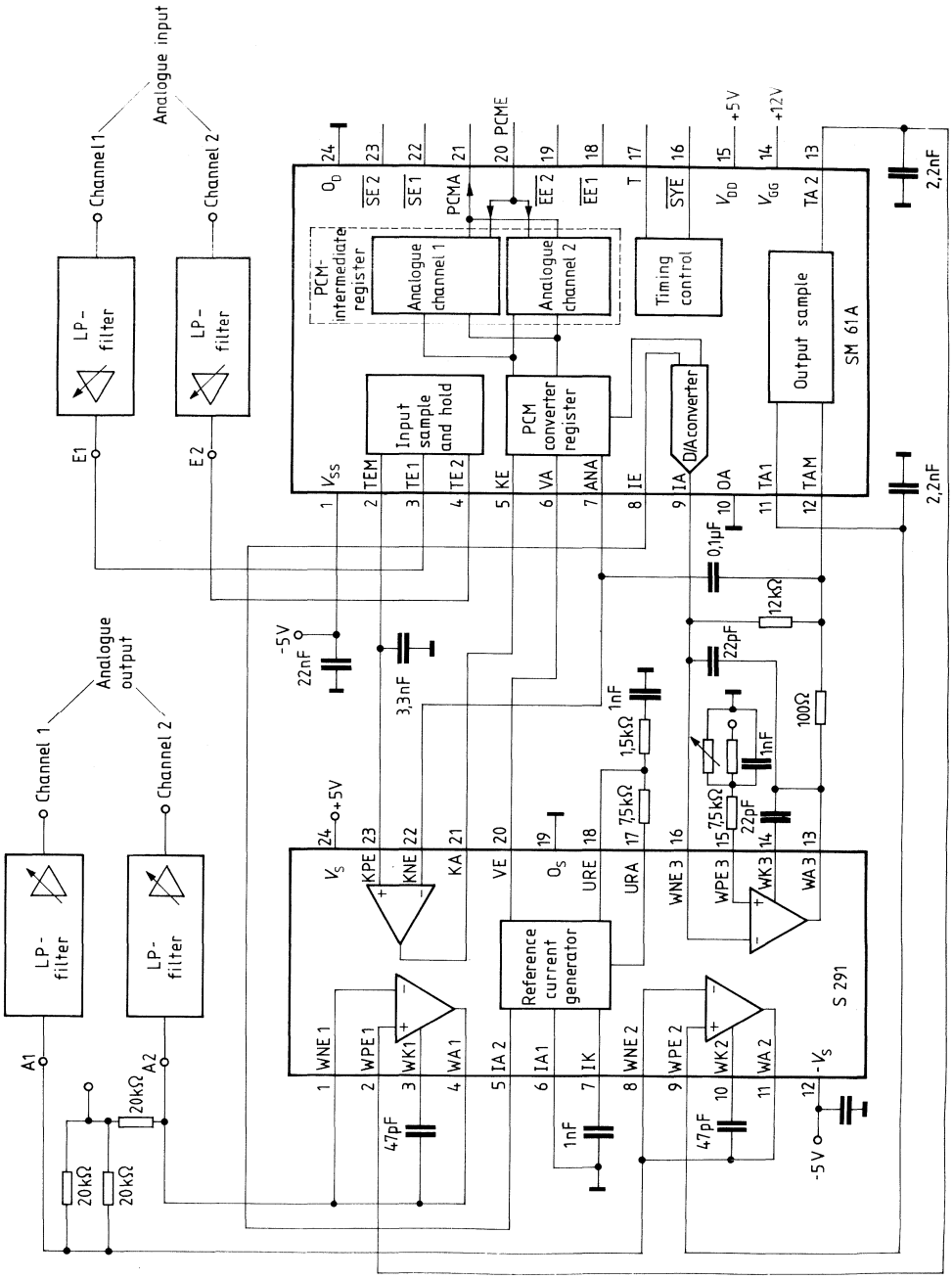


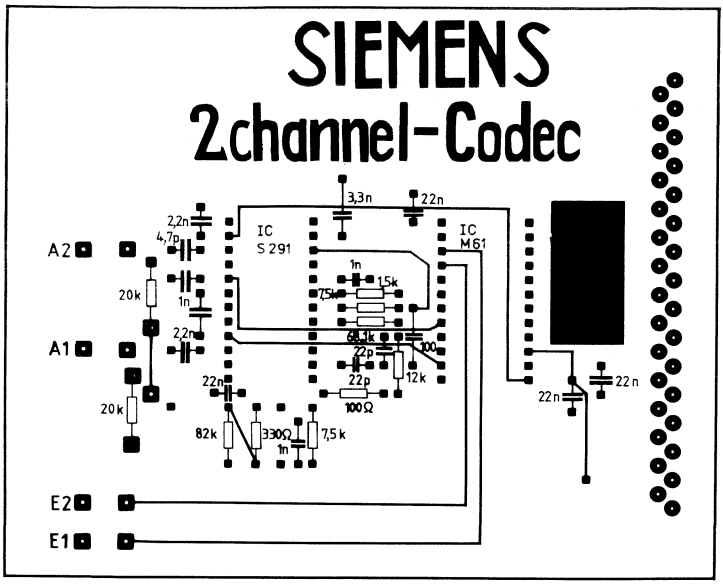
Figure 5: **Connections of PCM 2 – channel Codec (Evaluation – board and Filter)**

Connector assignment of the evaluation board

1	0 V analogue	11	not used	21	+12 V V_{GG}
2		12	$\overline{SE2}$	22	not used
3		13	$\overline{SE1}$	23	not used
4		14	PCM A	24	not used
5	+5 V V_{DD}	15	PCM E	25	not used
6	−5 V V_{SS}	16	$\overline{EE2}$	26	not used
7	0 V digital	17	$\overline{EE1}$	27	−5 V V_{SS}
8		18	clock T 2.048 MHz	28	not used
9		19	$\overline{SYE}$	29	+5 V V_{DD}
10		20	not used	30	not used
				31	not used

Connectors 5 and 29 (+5 V), as well as
6 and 27 (+5 V), to be connected
on the receptacle.

Make low-resistance connection of 0 V analogue with 0 V digital on the receptacle and with 0 V on the power supply.



Side for component parts

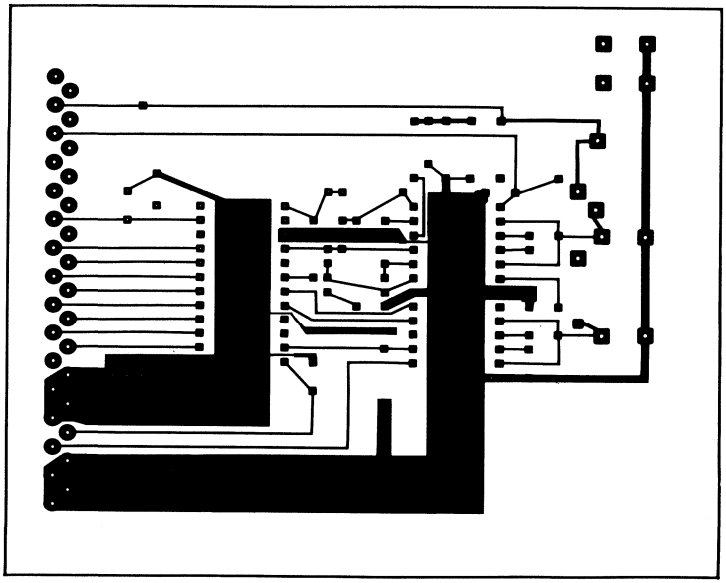


Figure 6

Decoding:

The 8-bit word received by the PCM 30/32-system through input PCME of the SM 61A is digitally expanded to 13-bit word width and applied to the D/A converter. The sumweighting-current at IA is put into the current/voltage converter of the bipolar circuit. The output voltage of this converter is connected to TAM, the input of the sample and hold portion. The resulting analogue voltage of the relevant channel is stored by the 2.2 nF capacitors at TA 1 or TA 2, respectively. Through the two OPs in the S 291 and the external low-pass filters it is assigned to the analogue output channels.

Coding:

The analogue audio signals of channels 1 and 2 are bandlimited by the input LP-filters and alternately applied to the positive input of the comparator through the input sample circuits (see timing diagram). The mutual 3.3 nF hold capacitor of the two channels is connected to output TEM of the sample circuit. For determining the sign of the sample value, the word 00000000 is generated in the converter register and put out as the analogue value zero. Consequently the weighting current IA = 0, and through the current/voltage converter the voltage at the negative comparator input is zero as well.

This way the comparator makes a decision about the sign and sets VA (sign output SM 61A) which is connected to VE (sign input S 291). Depending on VE the reference current is directed from IA2 (S 291) to IE (SM 61A). Following, the next bit = 1 is set, the new 8-bit PCM word is converted to 12 bit, the corresponding weighting current is directed to the current/voltage converter and the voltage proportional to the weighting current is compared with the sample value. The comparator decision determines, whether the bit concerned is maintained (if $V_{sample} \geqq V_{weight}$) or made zero. This process of approximation proceeds in steps up to the last bit, until the best approximation possible has been achieved. The final 8-bit word representing the sample value can be pushed out in the order of decreasing significance via PCM-A. In this process every second bit is inverted.

Timing

All control pulses are positioned inside a word-width within the channel pattern (≙ 8 bit PCM), synchronously with the pulse edge of the 2.048 MHz clock. For the synchronizing pulse $\overline{SYE}$, with a synchronous negative going edge, in principle the duration of one clock period would be sufficient. Its length is not restricted, however.

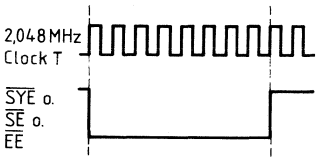


Figure 7: **Timing**

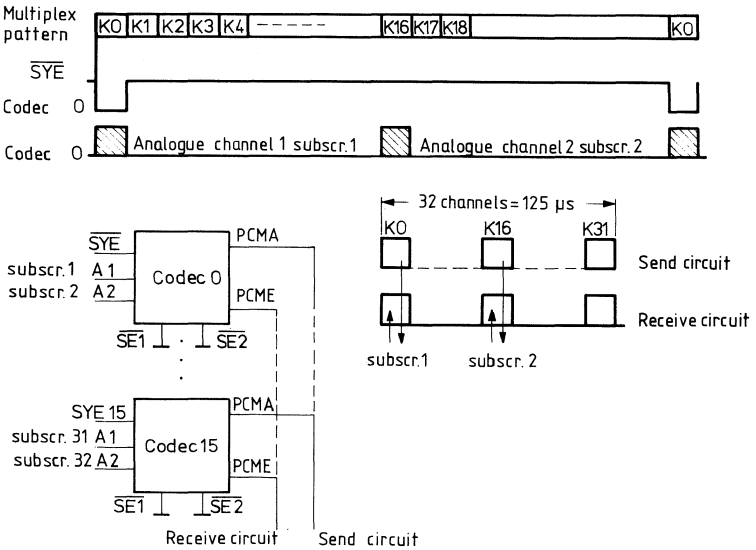


Figure 8: **Codec in short-way operation**

Decoupling in timing from the multiplex circuit. In this mode of operation, the send- and receive-pulses for an analogue channel have the same channel position. In principle the channel position of the synchronous pulse $\overline{SYE}$ may be chosen freely.

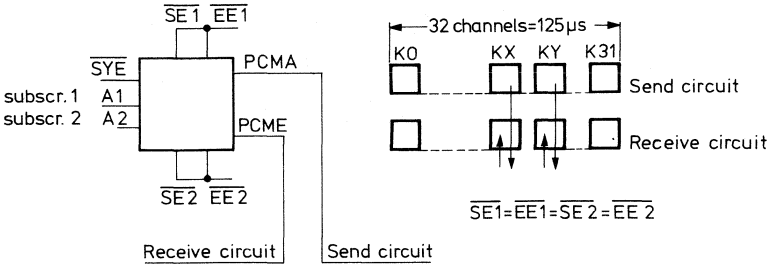


Figure 9: **Codec with decoupling in timing from the multiplex circuit**

However, differences in the propagation delay of a PCM-word will occur, depending on the choice of channel position of the $\overline{SYE}$. As an example, assume that $\overline{SYE}$ = $\overline{SE1}$ = $\overline{EE1}$ = KO in the channel pattern and $\overline{SE2}$ = $\overline{EE2}$ = K16. Then a PCM-word accepted from the receive-circuit of the multiplex system during the time interval KO will be transferred into the converter register and decoded 125 µs later, with the next synchronizing pulse during time interval KO (figure 7 refers). An equivalent situation exists for the PCM word accepted during time interval K 16 as well as for the PCM-words to be transmitted. However, if $\overline{SE1}$ = $\overline{EE1}$ = KO, $\overline{SE2}$ = $\overline{EE2}$ = K 16 and $\overline{SYE}$ = K1, the PCM-word received during KO is transferred into the converter register during interval K1, and the PCM-word receiving during K 16 is transferred during interval K 17. The same is true, correspondingly, for the PCM-words to be applied to any constellation of channel coordination wanted; they lead to the

Muldem-control for minimum propagation delay

In the case of an arrangement with mutual synchronizing pulse $\overline{SYE}$ for all 16 codec, e.g. channel KO, channels KO and K 16 would be consequently specified as codec-transfer-channels UE1 = KO and UE2 = K 16. (figure 17 refers). A control requirement is the condition that channel UE1 is assigned to an A2-participant ($\overline{SE2}$ = $\overline{EE2}$) and channel UE2 to an A1-participant ($\overline{SE1}$ = $\overline{EE1}$).

A muldem PC-board "PC" with n codes constitutes 2n channels of the multiplex system. If the control of the PC is done in such a way that the 2n control pulses ($\overline{SE}$ = $\overline{EE}$) of the PC are uniformly distributed throughout the timing frame (fig. 10), the above stated requirement will be satisfied if for all PC (number 32/2n) the A2-connections of the codecs are uniformly used for channels 0 . . . 15 and the A1-connections for channels 16 . . . 31.

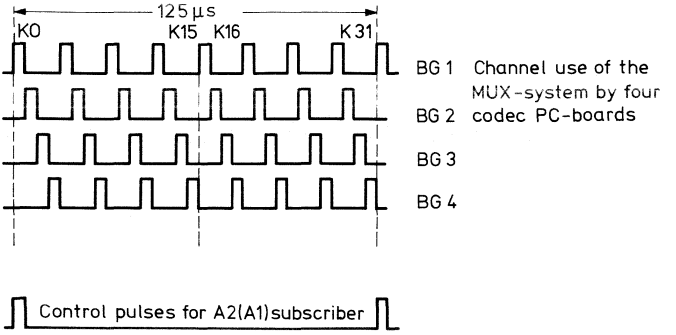


Figure 10: **Participant/channel correlation for minimum PCM propagation delay, with uniform channel distribution and mutual synchronizing pulse.**

In the case of a block-assignment of the multiplex channels per PC, i.e. immediately adjacent (figure 11), the distribution of connections for each PC must start with an A2-connection (remaining distribution optional), if also $\overline{SYE}$ = KO is provided. Thereby, for uniform PC, an A2-connection is also obtained with channel 16, and here a second synchronizing pulse $\overline{SYE}$ = KO is required. With two synchronizing pulses the following division appears advantageous: Codecs in the first half of the multiplexing frame get SYE = KO and the codecs in the second half $\overline{SYE}$ = K 16.

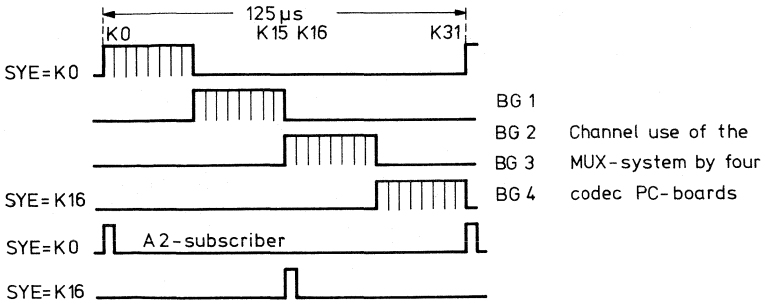


Figure 11: **Participant/channel correlation for minimum PCM propagation delay, with blockwise channel distribution**

A uniform synchronous pulse per PC or muldem offers the advantage of a better controllability of all converters operating synchronously; however, a second synchronous pulse in addition to the control pulses is required, and problems with the voltage supply (voltage drops, coupling) may occur. An alternate solution would be a distributed synchronization, involving the control pulses (figure 12).

The rule to be applied is simple:

$$\overline{SEY} = \overline{SE2} = \overline{EE2}$$

Hence, the synchronizing pulse is identical to the control pulse for the A2-participant and may be connected directly at the chip. All codecs will then operate with converter timings offset by two channels, with respect to each other.

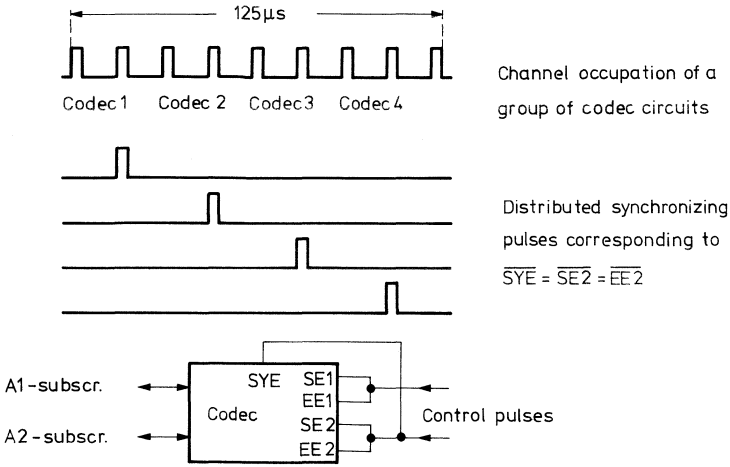


Figure 12: **Participant/channel correlation for minimum PCM propagation delay, in the case of distributed synchronization.**

Switching operation

In this mode of operation the transmitting and receiving line are identical for each multiplex system. Contrary to the modes of operation discussed so far, no coupling-matrix is required (establishing connection: Transmitting line participant X, receiving line participant Y; offset in timing transmitting channel participant X, receiving channel participant Y) to enable conversation of participants whose codecs are connected to the same transmitting and receiving lines.

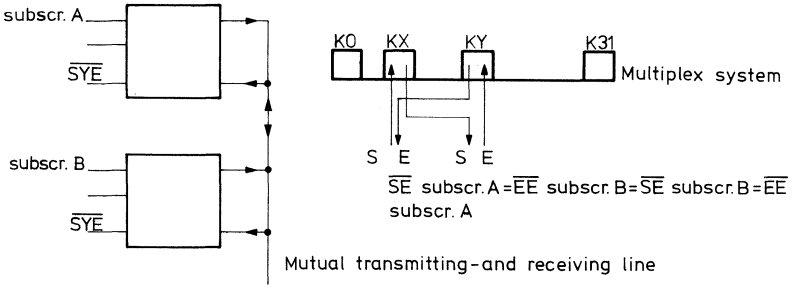


Figure 13: **Switching operation**

SM 61A1/S291A-System

PIN-Description: changes to SM 61A/S291-System

SM 61A:

ANKA: Autozero for comparator

ANWA: Autozero for current/voltage-converter

Power down mode (P_v <5 mW), if $\overline{EE1}$ = $\overline{EE2}$ = H-Level

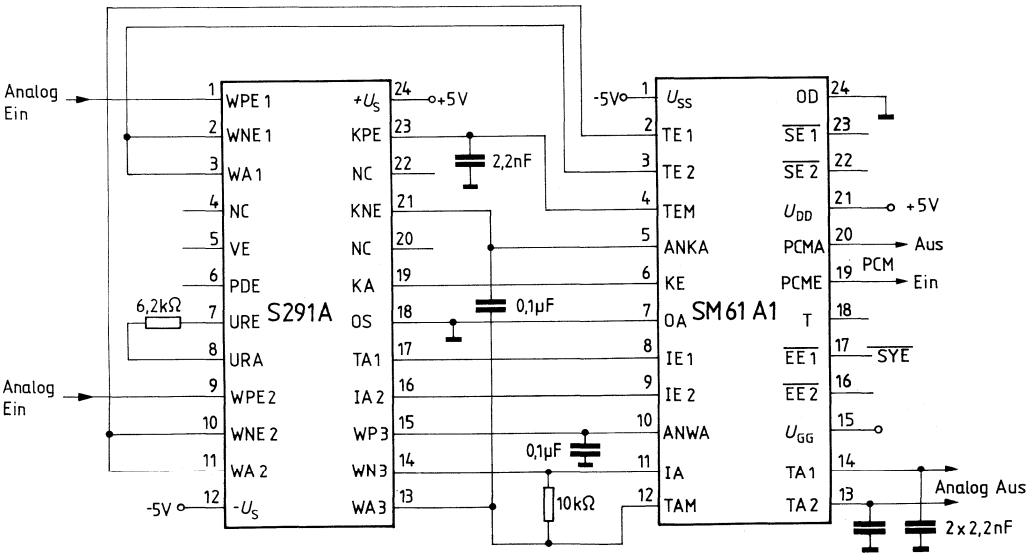
S 291A:

PDE: Power down enable (TTL-compatible)
L-Level: power down mode (P_v <1 mW)

NC: Not connected

Additional features:

Operational amplifiers internally compensated; input and output of comparator decoupled by NC-pins; power down mode of both chips, down to <10 mW autozero of comparator and current/voltage converter, i.e. no trimming necessary.



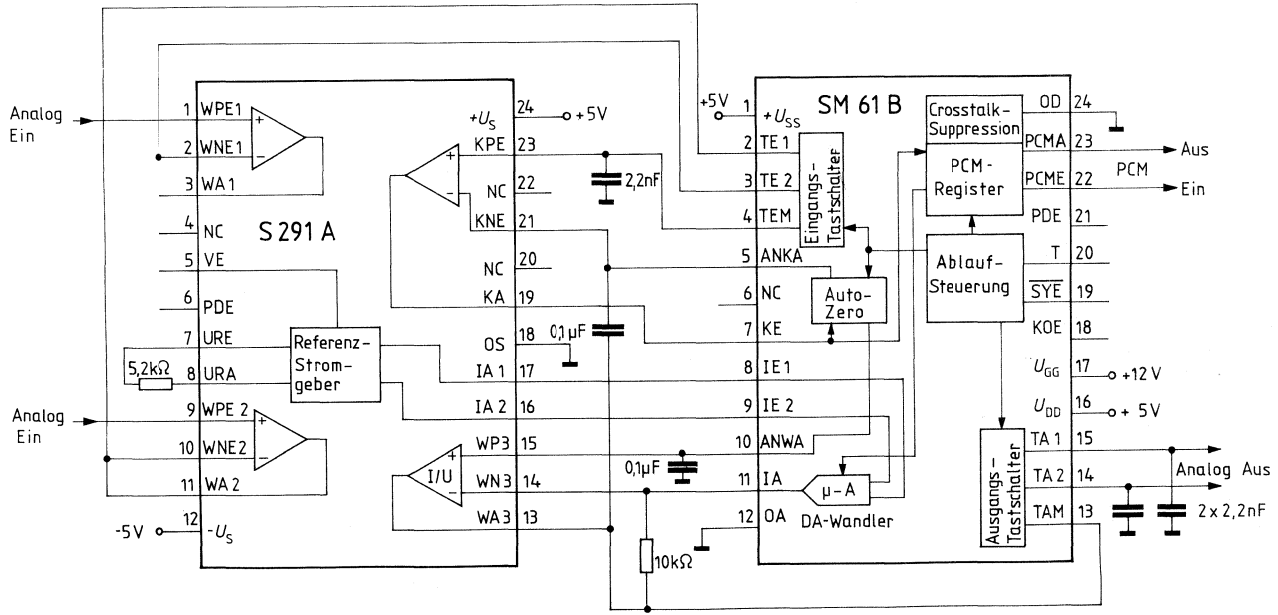
SM61B/S291A-System

Pin-Description: changes of SM61B to SM61A
PDE: Power Down Enable (P_v<5 mW)
KOE: switching from A-Law to μ-Law

Additional features:

First A-Law/μ-Law CODEC (switchable);
power down mode to <10 mW;
P_v <150 mW ≦75 mW/channel in active mode;

suppression of social crosstalk;
exchange register external for high system flexibility


Analog Ein
Analog Ein
S 291 A
1 WPE1
2 WNE1
3 WA1
4 NC
5 VE
6 PDE
7 URE
8 URA
9 WPE 2
10 WNE2
11 WA 2
12 -Us
-5V
5,2kΩ
Referenz-Strom-geber
+Us
24 +5V
KPE 23
NC 22
KNE 21
NC 20
KA 19
OS 18
IA 1 17
IA 2 16
WP3 15
WN3 14
WA3 13
I/U
2,2nF
0,1µF
0,1µF
10kΩ
+5V
SM 61 B
1 +Uss
2 TE 1
3 TE 2
4 TEM
5 ANKA
6 NC
7 KE
8 IE1
9 IE 2
10 ANWA
11 IA
12 OA
Eingangs-Tastschalter
Auto-Zero
µ-A
DA-Wandler
Crosstalk-Suppression
PCM-Register
Ablauf-Steuerung
Ausgangs-Tastschalter
OD 24
PCMA 23
PCME 22
PDE 21
T 20
SYE 19
KOE 18
UGG 17 +12 V
UDD 16 + 5V
TA 1 15
TA 2 14
TAM 13
Aus
PCM
Ein
Analog Aus
2 x 2,2nF